

A Programmable Crystal Substitute

A recent project to build a single side-band (SSB) detector for a venerable R-390A military receiver identified the need for a stable local oscillator capable of being switched between two frequencies. The complete SSB detector project is covered in *Tech Talk 10*.

Not so long ago, it would have been easy to build a simple oscillator using two crystals of the appropriate frequency. But crystals are not readily available now except for frequencies used in modern computer and similar circuits.

After considering various possible approaches, I decided to use a voltage controlled oscillator (VCO) locked to a standard commercial crystal using a phase-locked loop (PLL).

The PLL Approach

Figure 1 shows a typical PLL configuration. The phase detector compares the reference and signal waveforms continuously. Any phase difference is used to alter the VCO frequency so as to reduce the phase difference towards zero. Thus the relatively unstable VCO output is effectively locked to the much more stable crystal frequency.

While this is a good way to lock an unstable oscillator to a very stable reference, it can be made much more useful through the addition of signal and/or reference prescalars. For example, if the VCO is to oscillate at twice the reference frequency, then dividing the VCO output by two re-

sults in a signal at the phase detector that allows the loop to lock correctly.

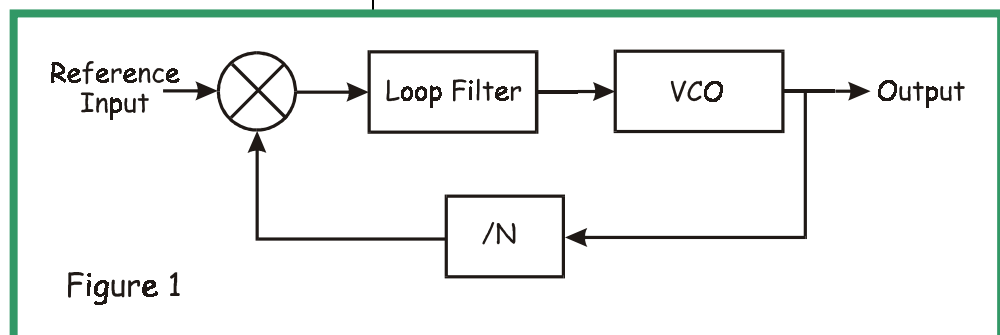
What this means is that the VCO can be locked to any multiple of the reference signal simply by selecting the appropriate scaling factor between the VCO and the phase detector. Using a programmable scalar provides selectable output frequencies that are multiples of the reference frequency.

By also scaling the reference frequency, the size of the VCO output frequency steps can be changed. This scaling factor will be called M (not shown in Figure 1). If, for example, it is desired that the VCO output be selectable in 1 kHz steps, the reference frequency needs to be scaled to 1 kHz, and the signal scalar can then be programmed to provide the VCO output in 1 kHz steps as well. By changing the reference scaling factor, other output step sizes can be realized. The output frequency is the phase detection frequency multiplied by the scalar N. The step size is the reference frequency divided by the scalar M.

The Reference and Signal Scalars

In my application I wanted two switch selected output frequencies: 458kHz and 452kHz.

I selected a phase detection frequency, thus step size, of 1 kHz and a reference crystal os-



cillator of 1 MHz (because it was a convenient frequency and I had some in my junk box!). Referring to Schematic 1, M thus needed to be 1000, and was achieved using three CD4029 up/down BCD decade scalars (U11, U12, U13). Note that the schematic does not show the power ground or supply connections to the various chips.

The VCO output needed to be divided by 452 or 458 to give the correct 1 kHz frequency at the phase detector. I used an additional three CD4029 BCD decade scalars (U3, U4 and U5), with CD4073 and CD4081 gates (U6 and U7) so that the signal scalars reset when the correct count was obtained.

With different gates, reference crystal and scaling factor M, this circuit could be used to generate virtually any frequency within the capability of the integrated circuits.

This may seem like a lot of parts for such a simple purpose, but the cost of everything in Schematic 1 is less than the cost of a single custom programmable oscillator.

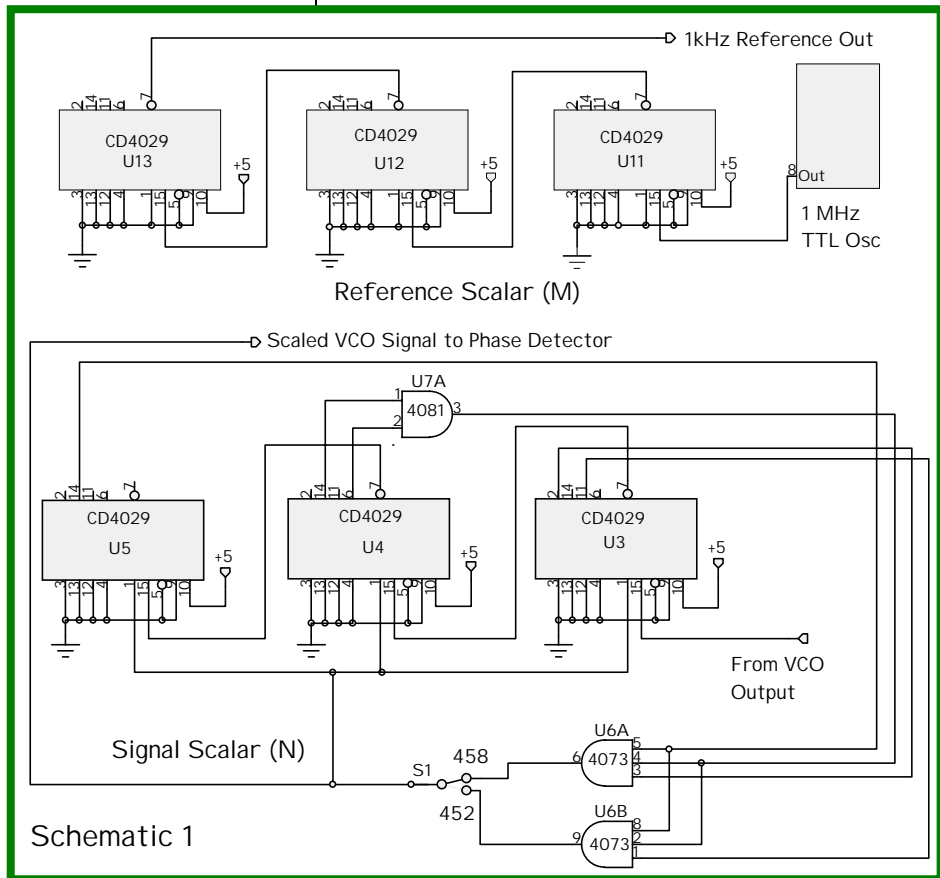
The Phase Detector and VCO

A CD4046B (U9) was used. It includes two phase detector circuits (only one of which is used in this application) and an independent VCO, all on a single chip.

There are other available chips that could be used instead of the CD4046B. For example, the MC14046B, made by ON Semiconductor appears to be a drop-in replacement.

A complete discussion of the CD4046B chip and how to apply it is beyond the scope of this article. Complete application information can be found on the Texas Instruments website by clicking [here](#).

The CD4046B has external components to

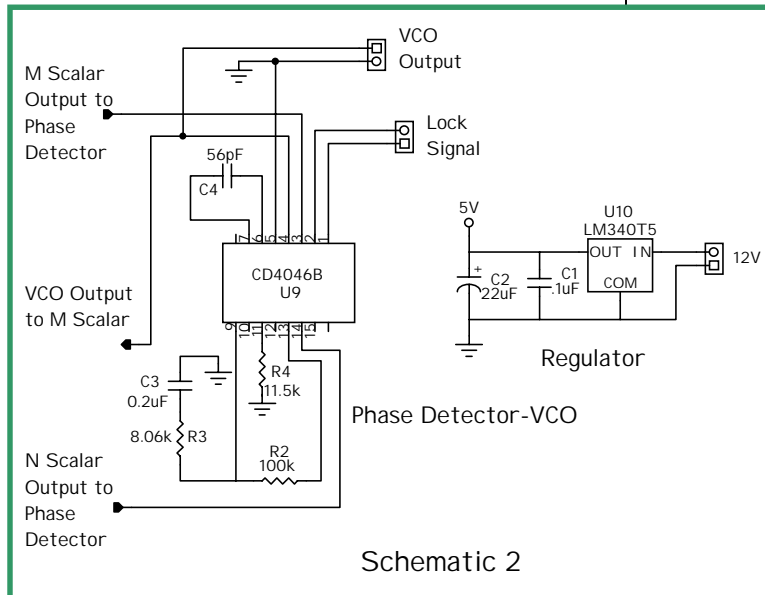


set the operating frequency (centre of the desired frequency range) and the characteristics of the loop filter.

The loop filter (a low pass RC filter) uses external components between the phase detector and the VCO. It determines the “tightness” of the lock between the VCO and the reference signal, and the frequency range over which a stable lock can be maintained. If the frequency centre is wrong, the phase detector is unable to bring the VCO to the desired frequency, so it is impossible to achieve a lock. If the loop filter is incorrect, the VCO may not lock or the lock may be unstable over part or all of the desired frequency range.

My impression is that the application information on how to determine the various component values should be considered a starting point at best. Another article I found suggests that the actual values in a particular application can vary by up to a factor of four from those determined from the TI application note.

Referring to Schematic 2, C4 and R4 set the centre frequency. C4 should be greater than 50pF and R4 greater than 10k but no greater than 1meg. As a guide, the higher R4 for a



Schematic 2

given C4, the lower the centre frequency. The higher C4, for a given R4, the lower the frequency. For a given R4 and C4, the frequency will increase as the supply voltage increases from 5V to 15V. The maximum usable centre frequency is likely to be about 1MHz.

The loop filter consists of R2, R3 and C3. The value of R2 is not critical. R3 is in the range of a tenth the value of R2. C3 is very important. I found that it was easiest to select the optimal value of C3 while observing the behaviour of the loop and the output waveform.

Other Issues

The CD4046B provides two pinouts that can be used to run a lock detect circuit. As my application requires only two frequencies, quite close together, I didn't include a lock detect.

The stability of the locked VCO will not be as good as the reference crystal. Phase noise is introduced due to inherent limits in the feedback loop design such that it cannot maintain a perfect lock. Also, jitter introduced by the scalar chains will also affect the output signal stability.

The output of this circuit is a square wave. For applications requiring a sine wave, an active filter is needed. *Tech Talk 10* includes a

design for a filter for use with the above circuit.

If it is adequate to be able to set the output frequency to multiples of 10kHz, or 100kHz, the scalar chains can be adjusted accordingly. If greater resolution than 1kHz is needed, additional scaling can be added.

The CD4046B will achieve lock within a few cycles at the comparison frequency. Thus, if you intend to switch between various frequencies using some variant of this circuit, the time to lock when the frequency is changed will be a few cycles multiplied by the scaling factor. Thus, this approach may not be useful if extremely fast frequency switching is needed. This is not an issue in this particular application.

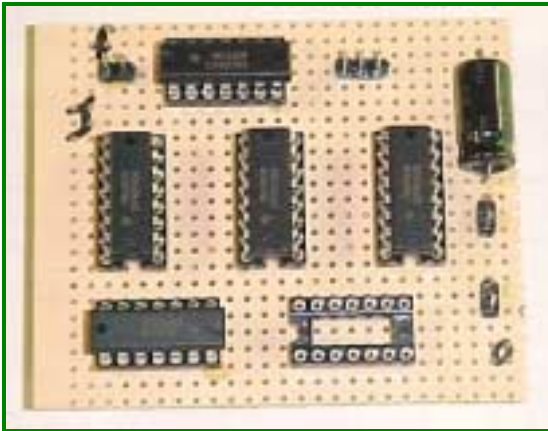
Schematic 2 also includes a voltage regulator to provide the 5V needed by the CMOS chips. The

CD4046B could be operated at higher voltages, but there was no advantage in doing so in this application.

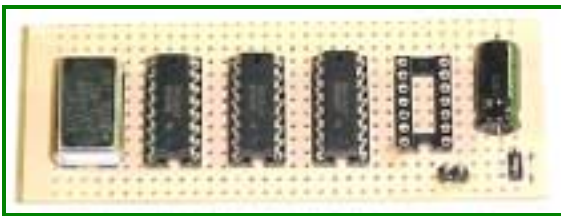
Parts List

| | |
|----------------------|-----------------------|
| C1 | 0.1uF ceramic |
| C2 | 22uF tantalum |
| C3 | 0.2uF ceramic |
| C4 | 56pF ceramic |
| J1 | Power connector |
| J2 | Lock signal connector |
| J12 | VCO Output |
| R2 | 100k, 1/4w |
| R3 | 8.06k, 1/4w |
| R4 | 11.5k, 1/4w |
| U1 | 1 MHz TTL Oscillator |
| U3,U4,U5,U11,U12,U13 | CD4029 |
| U6 | CD4073 |
| U7 | CD4081 |
| U9 | CD4046B |
| U10 | LM340T5 |
| S1 | SPDT switch |

Prototypes



The pictures show the VCO signal scalar (above) and reference scalar (below) prototype boards. As these are on separate boards, the power connection is bypassed on each board. The empty sockets were used for an alternate configuration. The three pin SIP connector on



the signal scalar board connects to an external SPDT frequency selection switch. A much smaller size could be achieved by using equivalent chips in a smaller form factor.
